Listing of the Claim:

This listing of the claims will replace all prior versions, and listings, of claims in the application. Claims 37 and 39 have been amended and the stray text that was erroneously introduced after claim 34 in the previous Amendment has been struck out.

Pending claims

1-22. (Cancelled.)

23.(Previously Presented) In an enclosed rectangularly shaped computer memory system that is less than 5.5 centimeters in width, less than 9.0 centimeters in length and less than 6.0 millimeters in thickness, and having an electrical connector along one side thereof, a combination comprising a plurality of substantially identical flash EEPROM integrated circuit chips, and a controller circuit interconnected between said electrical connector and said plurality of flash EEPROM integrated circuit chips.

24.(Previously Presented) The combination of claim 23 wherein said controller circuit includes means receiving from said connector a disk memory address in the form of head, cylinder, beginning sector and sector count designations for addressing corresponding memory locations within said flash EEPROM integrated circuit chips.

25.(Previously Presented) The combination of claim 24 wherein said plurality of flash EEPROM chips are each characterized by its storage capacity being divided into physical quadrants and each quadrant having a plurality of separately addressable sectors of memory cells, wherein a chip sector includes at least a number of cells equal to a number of bits in the disk sector, and further wherein said means receiving from said connector a disk memory address addresses the chips by designating an individual chip, its quadrant and a sector within that quadrant that corresponds with a disk sector address received from the connector.

26.(Previously Presented) The combination of claim 23 wherein said controller is characterized by interfacing through said connector with an industry standard IDE interface in order to translate signals received from a computer system bus according to that standard into signals that communicate with said plurality of EEPROM circuit chips.

27.(Previously Presented) In an enclosed package having an electrical connector carried thereby for interfacing with computer system signals that address disk memory by head number, cylinder number, and specific ones of a plurality of sectors that each contain a predetermined number of bytes, a mass storage system, comprising:

a plurality of flash EEPROM integrated circuit chips containing a large number of non-volatile memory cells arranged in physical quadrants on the chips and having separately addressable sectors of cells within the quadrants, the individual sectors having enough cells to store said predetermined number of bytes, and

a controller connected between said connector and said plurality of flash EEPROM integrated circuit chips in a manner to allow data to be written into said chips and to be read from said chips when a computer system is connected with said connector, said controller including means responsive to said computer system signals that address disk memory for addressing said plurality of EEPROM chips by corresponding chip numbers, quadrants and numbers of sectors, whereby the package of integrated circuit memory is addressed by a computer system as is disk storage memory.

28.(Previously Presented) The mass storage system according to claim 27 wherein said package is substantially rectangular in shape with a width of about 5.5 centimeters or less, a length of about 9.0 centimeters or less and a thickness of about 19 millimeters or less, and further wherein said electrical connector is mounted along one side thereof.

29.(Previously Presented) The mass storage system according to claim 27 wherein said package is a rectangularly shaped PC memory card with a width less than 5.5 centimeters,. a length less than 9.0 centimeters and a thickness of less than 6.0 millimeters, and further wherein said electrical connector is mounted along one side thereof.

30.(Previously Presented) The mass storage system according to claim 27 wherein said package has a width of about 5.4 centimeters, a length of about 7.3 centimeters and a thickness of about 19 millimeters or less, whereby said mass storage system is provided in a package that is substantially the same as an industry standard for a 1.8 inch hard disk drive.

31.(Previously Presented) The mass storage system according to claim 27

wherein said predetermined number of bytes is substantially 512.

32.(Previously Presented) The mass storage system according to claim 27 wherein said controller includes a plurality of temporary storage registers, a buffer data memory and a microprocessor, the registers and buffer memory being connected to be accessible both by a computer system through said connector and by said controller microprocessor, said microprocessor characterized by responding to a command written into one of said registers by an external computer system through the connector to carry out the command and thereafter writing into another one of said registers a status after the command has been executed.

33.(Previously Presented) The mass storage system according to claim 32 wherein said microprocessor is characterized by reading disk head, disk cylinder and disk sector addresses from others of said registers in response to a READ or a WRITE command in said one register, determining a corresponding address within the EEPROM chips, and then writing a completion status into said another one of said registers after data is read from or written into the EEPROM chip memory.

34.(Previously Presented) The mass storage system according to claim 33 wherein said microprocessor is additionally characterized by responding to a SEEK or a RESTORE command in said one register to immediately write a completion status into said another one of said registers.

~~a communication circuit including a serial portion extending through the host system and memory card connectors to transfer user data between the host system and said at least one accessed memory cell group.~~

35.(Previously Presented) In an enclosed rectangularly shaped computer memory system that is less than 5.5 centimeters in width, less than 9.0 centimeters in length and less than 6.0 millimeters in thickness, and having an electrical connector along one side thereof, a combination comprising a plurality of substantially identical flash EEPROM integrated circuit chips, and a controller circuit interconnected between said electrical connector and said plurality of flash EEPROM integrated circuit chips, wherein the transfer of data between said electrical connector and said plurality of flash EEPROM integrated circuit chips includes a serial transfer portion.

36.(Previously Presented) The combination of claim 35 wherein said controller circuit includes means receiving from said connector a disk memory address in the form of head, cylinder, beginning sector and sector count designations for addressing corresponding memory locations within said flash EEPROM integrated circuit chips.

37.(Presently Amended) The combination of claim 36 wherein said plurality of flash EEPROM chips are each characterized by its storage capacity being divided into physical quadrants and each quadrant having a plurality of separately addressable sectors of memory cells, wherein a chip sector includes at least a number of cells equal to a number of bits in the disk sector, and further wherein ~~said~~ an EEPROM addressing means addresses the chips by designating an individual chip, its quadrant and a sector within that quadrant that corresponds with a disk sector address received from the connector.

38.(Previously Presented) The combination of claim 35 wherein said controller is characterized by interfacing through said connector with an industry standard IDE interface in order to translate signals received from a computer system bus according to that standard into signals that communicate with said plurality of EEPROM circuit chips.

39.(Presently Amended) In an enclosed package having an electrical connector carried thereby for interfacing with computer system signals including computer address signals that address disk memory by head number, cylinder number, and specific ones of a plurality of sectors that each contain a predetermined number of bytes, a mass storage system, comprising:

a plurality of flash EEPROM integrated circuit chips containing a large number of non-volatile memory cells arranged in physical quadrants on the chips and having separately addressable sectors of cells within the quadrants, the individual sectors having enough cells to store said predetermined number of bytes, and

a controller connected between said connector and said plurality of flash EEPROM integrated circuit chips in a manner to allow data to be written into said chips and to be read from said chips when a computer system is connected with said connector, said controller including means responsive to said computer address signals for addressing said plurality of EEPROM chips by corresponding chip numbers, quadrants and numbers of sectors,

whereby the package of integrated circuit memory is addressed by a computer system as is disk storage memory, wherein the transfer of said data between said computer system and said plurality of EEPROM chips includes a serial transfer portion.

40.(Previously Presented) The mass storage system according to claim 39 wherein said package is substantially rectangular in shape with a width of about 5.5 centimeters or less, a length of about 9.0 centimeters or less and a thickness of about 19 millimeters or less, and further wherein said electrical connector is mounted along one side thereof.

41.(Previously Presented) The mass storage system according to claim 39 wherein said package is a rectangularly shaped PC memory card with a width less than 5.5 centimeters,. a length less than 9.0 centimeters and a thickness of less than 6.0 millimeters, and further wherein said electrical connector is mounted along one side thereof.

42.(Previously Presented) The mass storage system according to claim 39 wherein said package has a width of about 5.4 centimeters, a length of about 7.3 centimeters and a thickness of about 19 millimeters or less, whereby said mass storage system is provided in a package that is substantially the same as an industry standard for a 1.8 inch hard disk drive.

43.(Previously Presented) The mass storage system according to claim 39 wherein said predetermined number of bytes is substantially 512.

44.(Previously Presented) The mass storage system according to claim 39 wherein said controller includes a plurality of temporary storage registers, a buffer data memory and a microprocessor, the registers and buffer memory being connected to be accessible both by a computer system through said connector and by said controller microprocessor, said microprocessor characterized by responding to a command written into one of said registers by an external computer system through the connector to carry out the command and thereafter writing into another one of said registers a status after the command has been executed.

45.(Previously Presented) The mass storage system according to claim 44 wherein said microprocessor is characterized by reading disk head, disk cylinder and disk sector addresses from others of said registers in response to a READ or a WRITE command in said one

register, determining a corresponding address within the EEPROM chips, and then writing a completion status into said another one of said registers after data is read from or written into the EEPROM chip memory.

46.(Previously Presented) The mass storage system according to claim 45 wherein said microprocessor is additionally characterized by responding to a SEEK or a RESTORE command in said one register to immediately write a completion status into said another one of said registers.